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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Applicant: YAMADA et al

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Filing Date: November 27, 2001

Date: April 18, 2002 Page 1 of 1

Examiner: to be assigned | Group Art Unit: 2812

U.S. PATENT DOCUMENTS

Examiner's Initials*		Document Number	Date MM/YYYY	Name (Family Name of First Inventor)	Class	Sub Class	Filing Date (if appropriate)
MC	AR	5,929,476	07/1999	PRALL			
	BR						
	CR						
	DR						
	ER						
	FR						
	GR						
	HR						
	IR						

FOREIGN PATENT DOCUMENTS

		Document Number	Date MM/YYYY	Country	Inventor Name		English Abstract		Translation Readily Available	
							Enclosed	No	Enclose	No
	JR									
	KR									
	LR									
	MR									
	NR									
	OR									
	PR									
	QR									
	RR									
	SR									

OTHER (Including in this order Author, Title, Periodical Name, Date, Pertinent Pages, etc.)

MC	TR	Patent Abstracts of Japan, Publ. No. JP 01 158768, Vol. 013, No. 429, 1989
MC	UR	Patent Abstracts of Japan, Publ. No. JP 01 147860, Vol. 013, No. 407, 1989
MC	VR	Rupp et al., "Extending trench DRAM technology to 0.15 μm groundrule and beyond", IEDM Technical Digest, 1999, pg. 33-36
MC	WR	Gruening et al., "A novel trench DRAM cell with a VERtIcal access transistor and BuriEd STrap (VERI BEST) for 4Gb/16Gb", IEDM Technical Digest, 1999, pg. 25-28
MC	XR	"High density vertical DRAM cell", IBM Technical Disclosure Bulletin, Vol. 29, No. 5, 1986, pg. 2335-2340
	YR	

Examiner [signature] Date Considered: 7/5/02

*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.